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10/609,091	06/27/2003	Vinson Chan	174 / 258	7580

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,091	CHAN ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because some of the hand writing in the drawing are not clear. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Venkata et al. (US 6,854,044).

- With regard claim 1, Venkata et al. discloses a Byte alignment circuitry (Fig.1 element 50) comprising:

  a data input (Fig.1 element 42);

  a control input (Fig.1 element 34);

  a special character selection input indicating which special character is to be used for byte alignment (Fig.1 element 34 and column 3 lines 8-17); and

  a special character status output indicating which special character was used to align the byte boundaries (Fig.1 element 54 and column 3 lines 8-17); and

  a data output (Fig.1 element 52).

- With regard claim 2, Venkata et al. further discloses wherein the data input is one of a plurality of parallel data inputs (Fig.1 element 42).
- With regard claim 3, Venkata et al. further discloses wherein the plurality is the number of bits in a byte (Fig.1 element 42 and column 2 lines 63-64).
- With regard claim 4, Venkata et al. further discloses wherein the data output is one of a plurality of parallel data outputs (Fig.1 element 52).
- With regard claim 5, Venkata et al. further discloses wherein the plurality is the number of bits in a byte (Fig.1 element 52 and column 2 lines 63-64).

- With regard claim 6, Venkata et al. further wherein successive aligned bytes are output one after another via the data outputs (column 1 lines 8-10 and column 7 lines 50-52).
- With regard claim 7, Venkata et al. further discloses a clock input (Fig.1 element 44).
- With regard claim 8, which is a digital processing system (Fig.5 element 502) related to claim 1, Venkata et al. further discloses

  a processing circuitry (Fig.5 element 504);

  a memory coupled to the processing circuitry (Fig.5 element 506); and

  byte alignment circuitry (Fig.5 element 10 and Fig.1 element 10) as defined in claim 1 coupled to the processing circuitry and the memory.
- With regard claim 9, Venkata et al. further discloses a printed circuit board (Fig.5 element 530 and column 6 lines 64-66) on which is mounted byte alignment circuitry (Fig.5 element 10 and Fig.1 element 10) as defined in claim 1.
- With regard claim 10, Venkata et al. further discloses a memory (Fig.5 element 506) mounted on the printed circuit board and coupled to the byte alignment circuitry (Fig.5 element 10 and Fig.1 element 10).
- With regard claim 11, Venkata et al. further discloses processing circuitry (Fig.5 element 504) mounted on the printed circuit board and coupled to the byte alignment circuitry.

- With regard claim 12, Venkata et al. discloses a circuitry for receiving and byte-aligning data comprising:

  byte alignment circuitry (Fig.1 elements 10 and 50) that uses a first special character selected by a special character selection signal to detect byte boundaries in received data (Fig.1 element 34, SYNC_PAT, and column 3 lines 8-17), and

  aligns the byte boundaries when enabled by a control signal (Fig.1 element ENC_DET) to subsequently output byte-aligned data (Fig.1 element 34 and column 3 lines 8-17 and column lines 40-46) and a special character status signal indicative of the special character used to align the byte boundaries (Fig.1 element 54 and column 3 lines 8-17); and

  utilization circuitry responsive to outputs of the byte alignment circuitry and selectively providing said control signal and said special character selection signal (Fig.1 element 60-62 and column 1 lines 54-64, column 3 lines 33-57 and column 8 lines 17-19).

- With regard claim 13, Venkata et al. further discloses wherein the byte-aligned data is output in parallel form (Fig.1 element 42).

- With regard claim 14, Venkata et al. further discloses wherein said utilization circuitry comprises programmable logic circuitry (Fig.1 element 30).

- With regard claim 15, Venkata et al. further discloses wherein said byte alignment circuitry outputs a pattern detect signal indicative of the presence of

byte aligned data (Fig.1 element 56, PATTERN_DETECT); and said pattern detect signal causes said utilization circuitry to disable said control signal (column 3 line 33 – column 4 line 60, especially column 3 line 58-62).

- With regard claim 16, Venkata et al. further discloses wherein said byte alignment circuitry automatically prevents alignment to subsequently received data containing byte boundary data after the byte boundaries have already been aligned (column 3 line 33 – column 4 line 60, especially column 3 line 58-62).

- With regard claim 17, Venkata et al. further discloses wherein said byte alignment circuitry provides data representing said first special character to said
utilization circuitry (column 3 lines 33-39).

- With regard claim 18, Venkata et al. further discloses wherein said special character select signal can instruct said byte alignment circuitry to use a second special character to detect the byte boundaries in received data (column 3 line 33 – column 4 line 60, where examiner considers that the second special character is no different from the first special character).

- With regard claim 19, Venkata et al. further discloses wherein said byte alignment circuitry re-aligns the byte boundaries using said second special character when enabled by said control signal (column 4 lines 8-27).

- With regard claim 20, Venkata et al. discloses Circuitry for receiving and byte-aligning data comprising:

  byte alignment circuitry that processes received data and outputs byte-aligned data after byte boundaries are aligned (Fig.1 element 50 and column 3 lines 8-57), said byte alignment circuitry further comprising:

  special character detection circuitry that detects a selected special character in the received data, said selected special character is selected based on a selection signal (column 3 line 8-32 and Fig.2 element 120 and Fig.4a element 206); and

  boundary adjustor circuitry that sets the byte boundaries when said selected special character is detected and criteria are met (column 3 line 33-35 and Fig.4a element 210); and

  utilization circuitry that receives the outputs of said byte alignment circuitry (Fig.1 element 60-62 and column 1 lines 54-64, column 3 lines 33-57 and column 8 lines 17-19).

- With regard claim 21, Venkata et al. further discloses wherein said selection signal is hardwired to permanently select a particular selected special character (column 3 lines 8-12).

- With regard claim 22, Venkata et al. further discloses wherein said utilization circuitry provides said selection signal to select a particular special character

(column 3 lines 8-12, where the special character SYNC_PAT is selected and provided to alignment logic circuitry 50 through lead 34).

- With regard claim 23, Venkata et al. further discloses wherein said byte alignment circuitry disables said boundary adjustor circuitry independent of a control signal (Fig.4a element 214 and column 6 lines 25-34).

- With regard claim 24, Venkata et al. further discloses wherein said utilization circuitry enables said boundary adjustor circuitry by providing a control signal to said byte alignment circuitry (column 3 lines 8-17).

- With regard claim 25, Venkata et al. further discloses wherein said byte alignment circuitry further comprising constructor circuitry (Fig.5 element 10 and Fig.1 element 10, where the byte alignment circuitry 50 is included in the system 10 of Fig.1).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang